Claims

What is claimed is:

1. A method for transferring data between a host device and a storage medium, comprising:

receiving from the host device a command to transfer data between the host device and the storage medium;

storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out of the buffer;

modifying a value contained in the first register in response to a transfer of a data unit into the buffer; and

modifying a value contained in the first register in response to a transfer of a data unit out of the buffer.

2. The method of claim 1, further comprising:

storing in a second register a value for incrementing a value contained in the first register; and

incrementing a value contained in the first register by the value contained in the second register.

3. The method of claim 1, further comprising:

storing in a third register a value for decrementing a value contained in the first register; and

decrementing a value contained in the first register by the value contained in the third register.

4. The method of claim 1, further comprising:

storing in a fourth register an address representing a location in the buffer where data is being transferred between the buffer and the host device; and

storing in a fifth register an address representing a location in the buffer where data is being transferred between the buffer and the storage medium.

5. The method of claim 4, further comprising:

storing in a sixth register an address representing a beginning of the buffer; and

storing in a seventh register an address representing an end of the buffer.

6. The method of claim 5, further comprising:

storing in an eighth register a value representing a storage capacity of the buffer.

7. The method of claim 1, wherein the host device is a computer.

8. The method of claim 1, wherein the storage medium comprises non-volatile semiconductor memory.

9. The method of claim 1, further comprising:

implementing the method via an application specific integrated circuit (ASIC).

10. A data transfer system for transferring data between a host device and a storage medium, comprising:

a host interface that receives from the host device a command to transfer data between the host device and the storage medium;

a buffer that temporarily stores data that is transferred between the host device and the storage medium;

a first register that stores a value for tracking a number of data units that have been transferred into the buffer but that have not yet been transferred out of the buffer;

a second register that stores a value for incrementing a value contained in the first register; and

a third register that stores a value for decrementing a value contained in the first register.

11. The data transfer system of claim 10, wherein the data transfer system is configured to modify a value contained in the first register in response to a transfer of a data unit between the buffer and the host device.

12. The data transfer system of claim 11, wherein the data transfer system is configured to modify a value contained in the first register in response to a transfer of a data unit between the buffer and the storage medium.

13. The data transfer system of claim 10, wherein the data transfer system is configured to increment a value contained in the first register by the value contained in the second register.

14. The data transfer system of claim 13, wherein the data transfer system is configured to decrement a value contained in the first register by the value contained in the third register.

15. The data transfer system of claim 10, further comprising:

a fourth register that stores an address representing a location in the buffer where data is being transferred between the buffer and the host device; and

a fifth register that stores an address representing a location in the buffer where data is being transferred between the buffer and the storage medium.

16. The data transfer system of claim 15, further comprising:

a sixth register that stores an address representing a beginning of the buffer; and

a seventh register that stores an address representing an end of the buffer.

17. The data transfer system of claim 16, further comprising:

an eighth register that stores a value representing a storage capacity of the buffer.

18. The data transfer system of claim 10, wherein the data transfer system is an application specific integrated circuit (ASIC).

19. A method for transferring data between a host device and a storage medium, comprising:

receiving from the host device a command to transfer data between the host device and the storage medium;

storing in a first register a value for determining a buffer's fullness;

incrementing a value contained in the first register by a value contained in a second register; and

decrementing a value contained in the first register by a value contained in a third register.

20. The method of claim 19, further comprising:

incrementing a value contained in the first register by the value contained in the second register in response to a data transfer into the buffer.

21. The method of claim 19, further comprising:

decrementing a value contained in the first register by the value contained in the third register in response to a data transfer out of the buffer.

22. An application specific integrated circuit (ASIC) for transferring data between a host device and a storage medium, comprising:

a buffer that temporarily stores data that is transferred between the host device and the storage medium;

a first register that stores a value for determining the buffer's fullness;

a second register that stores a value for incrementing a value contained in the first register; and

a third register that stores a value for decrementing a value contained in the first register.

23. The ASIC of claim 22, wherein the data transfer system is configured to increment a value contained in the first register by the value contained in the second register in response to a data transfer into the buffer.

24. The ASIC of claim 22, wherein the data transfer system is configured to decrement a value contained in the first register by the value contained in the third register in response to a data transfer out of the buffer.